REMARKS

Claims 1-21 are pending in the present application and have been represented without amendment for reconsideration by the Examiner. Claims 1 and 12 are independent. Reconsideration of this application, in view of the following remarks, is respectfully requested.

Rejection Under 35 U.S.C. § 103

Claims 1-5, 7, 9-16, 18, 20 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Katoh et al., U.S. Patent No. 6,173,433. Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Katoh et al., U.S. Patent No. 6,173,433 in view of Cariffe et al., U.S. Patent No. 6,201,548. Claims 8 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Katoh et al. in view of Hernandez et al., U.S. Patent No. 4,686,522. These rejections are respectfully traversed.

The present invention is directed to a method and apparatus for creating a logical network by inserting a plurality of objects into a working area on a computer display. Independent claim 1 exemplifies the method of the present invention and recites a combination of steps including "displaying an existing network in said working area," "identifying at least one subarea of the working area where an object is insertable into said network," identifying what type of object that can be inserted into the network in said

subarea" and "displaying an extended network where an additional object of the type that is indicated in association with the selected subarea is inserted into the selected subarea."

Independent claim 12 exemplifies the apparatus of the present invention and recites a combination of elements including "means for displaying an existing network in said working area," "means for identifying at least one subarea of the working area where an object is insertable into said network," "means for identifying what type of object that can be inserted into the network in said subarea" and "means for displaying an extended network where an additional object of the type that is indicated in association with the selected subarea is inserted into the selected subarea."

The method and apparatus of the present invention is illustrated most clearly by Figs. 4a and 4b of the present invention. Specifically, an existing network 20 is illustrated in Fig. 4a, while an extended network 20' is illustrated in Fig. 4b. Applicants respectfully submit that the references relied on by the Examiner fail to teach or suggest the presently claimed invention.

In particular, referring to the Katoh et al. reference, this reference is related to the design of optical waveguides between circuit parts. A waveguide between circuit parts as disclosed by Katoh et al. cannot be considered a "logical network," as recited in the independent claims of the present invention. A logical network is a flow of information, such as a control program, where the result is dependent upon the information entered. A waveguide, on the other hand, merely guides the incident light to another location, possibly altering its characteristics, but without any logical decisions being made during the process.

Therefore, the need for a method according to the invention, ensuring a logically correct network, is not required when designing a waveguide.

Since Katoh et al. is not directed to the design of a logical network, Applicants submit that the Katoh et al. reference fails to anticipate independent claims 1 and 12 of the present invention for at least this reason.

In Katoh et al., a computer system automatically generates a virtual path between two connection terminals that have been specified by the user. The computer system does not assist the user in selection of different circuit parts, but merely determines a propagation path between selected parts, and provides a collection of standard parts, that can be tuned by the user to realize the calculated waveguide. (See column 4, lines 30-43, column 4, lines 57-63).

The system in Katoh et al. does not identify subareas of the working area where an object is insertable into a network. On the contrary, the user himself must indicate between which points a path should be calculated. In addition, the system in Katoh et al. does not identify what type of object that can be inserted into the network. Any such identification must be performed by the user himself. In other words, in Katoh et al., the user indicates two circuit parts that are to be connected together and the computer automatically determines the appropriate waveguide to connect the two circuit parts together. This can be clearly understood from column 4, lines 33-35 of Katoh et al., which states "a propagation path for the optical waveguides or microwaves is automatically determined [by the computer]." (emphasis added).

Furthermore, Katoh et al. does not disclose visually indicating an insertable object type in association with each subarea. The examiner makes reference to column 4, lines 35-38, and states that the Katoh et al. system generates a plurality of possible paths. However, as mentioned above, the computer automatically determines the appropriate waveguide. In view of this, there is no visual indication in Katoh et al. of an object type as recited in independent claims 1 and 12 of the present invention. In other words, in Katoh et al., the possible paths are not visually indicated, but only generated as part of a process of finding the optimal path (See column 18, lines 27-32).

According to the Examiner, column 16, lines 22-24 of Katoh et al. disclose how input is received from the user selecting a subarea. In fact, this section describes how the user indicates, by using a "determination indication button 705" that the user has completed a manual selection of a standard part. The system then moves on to determining the parameters of this part, in a partly automatic way (See column 16, lines 27-41).

To summarize, Kato et al. describes an entirely different process compared to the present invention. The purpose of the present invention is to facilitate the insertion of objects into a logical network in a correct way, e.g. resulting in a compilable control program. Katoh et al., on the other hand, is directed towards assisting a user to design optical waveguides between circuit parts, the selection and positioning of which have already been performed by the user.

With regard to dependent claims 2-5, 7, 9-11, 13-16, 18, 20 and 21, Applicants respectfully submit that these claims are allowable due to their respective dependence

upon allowable independent claims 1 and 12, as well as due to the additional recitations in these claims.

In view of the above, Applicants respectfully submit that the Katoh et al. reference fails to anticipate independent claims 1-5, 7, 9-16, 18, 20 and 21 of the present invention. Reconsideration and withdrawal of the Examiner's rejection under 35 U.S.C. § 102(e) are therefore respectfully requested.

With regard to the Examiner's reliance on the Cariffe et al. reference and the Hernandez et al. reference, these references have been relied on to disclose graphically outlining a subarea and changing the appearance of a cursor, respectively. There is no disclosure in either of the Cariffe et al. or Hernandez et al. references of "displaying an extended network where an additional object of the type that is indicated in association with the selected subarea is inserted into the selected subarea" as recited in independent claims 1 and 12 of the present invention. Accordingly, these references fail to make up for the deficiencies of Katoh et al.

It should be noted that the Examiner references the Wright reference on page 6, paragraph 14 of the Examiner's Office Action. However, the Examiner does not mention the Wright reference in the statement of the rejection. It is believed that the inclusion of the Wright reference is a typographical error; however, clarification is requested.

In view of the above remarks, Applicants respectfully submit that claims 1-21 clearly define the present invention over the references relied on by the Examiner. Accordingly,

reconsideration and withdrawal of the Examiner's rejections under 35 U.S.C. §§ 102 and 103 are respectfully requested.

CONCLUSION

All the stated grounds of rejection have been properly traversed and/or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently pending rejections and that they be withdrawn.

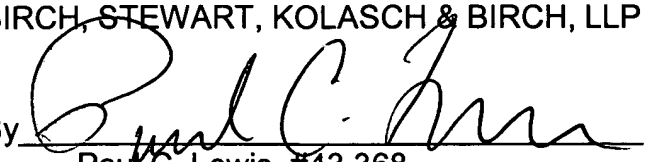
It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Paul C. Lewis, Registration No. 43,368 at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By 
Paul C. Lewis, #43,368

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

PCL/cl
0104-0345P